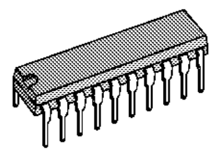
SGS-THOMSON MICROELECTRONICS

L6374

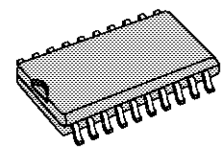
INDUSTRIAL QUAD LINE DRIVER

ADVANCE DATA

- FOUR INDEPENDENT LINE DRIVERS WITH 100 mA UP TO 35V OUTPUTS
- INPUT SIGNALS BETWEEN -7V AND +35V, WITH PRESETTABLE THRESHOLD
- PUSH-PULL OUTPUTS WITH THREE STATE CONTROL AND TRUE ZERO CURRENT BETWEEN V_S AND GROUND
- CURRENT LIMITING ON EACH OUTPUT EFFECTIVE IN THE FULL "GROUND TO V_S" OUTPUT VOLTAGE RANGE
- OUTPUT VOLTAGE CLAMP TO V_S AND TO GROUND
- OVERTEMPERATURE AND UNDERVOLTAGE PROTECTIONS
- DIAGNOSTIC FOR OVERTEMPERATURE, UNDERVOLTAGE AND OVERCURRENT
- PRESETTABLE DELAY FOR OVERCURRENT DIAGNOSTIC
- HIGH SPEED OPERATION: UP TO 300kHz WITH 35V SWING



POWERDIP 16+2+2



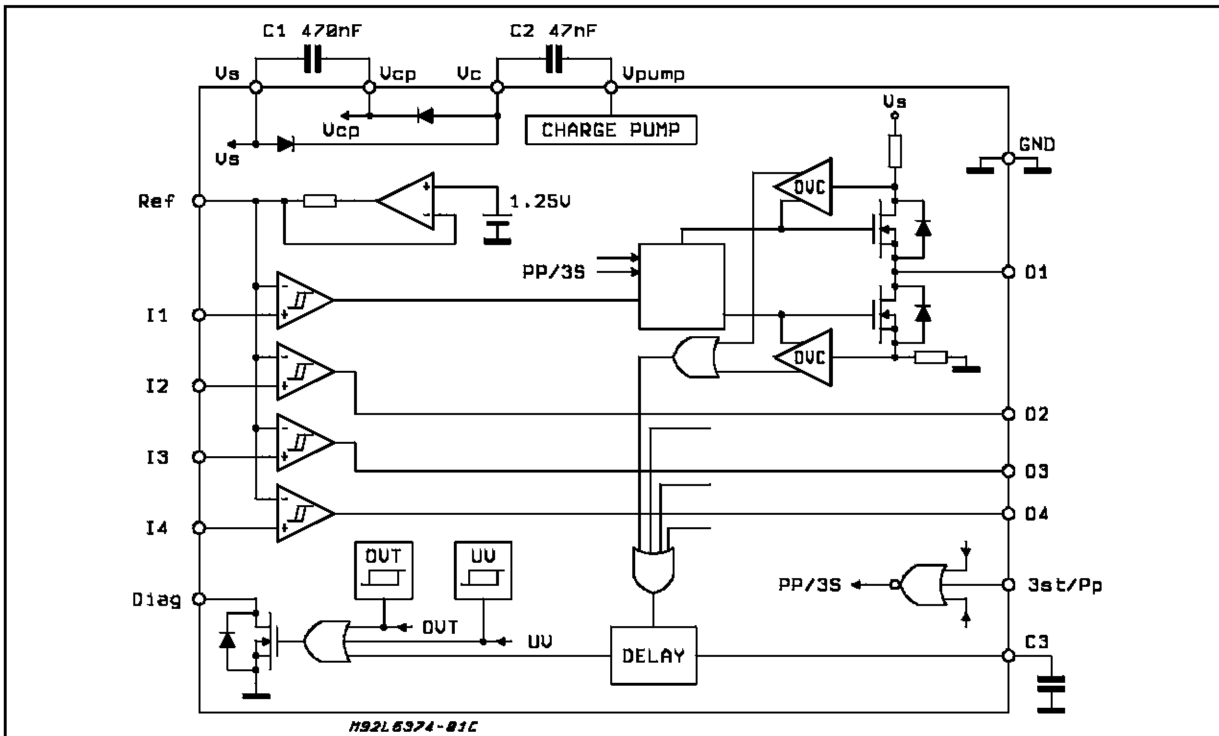
SO 16+2+2

ORDERING NUMBER: L6374DP (POWERDIP 16+2+2)
L6374FP (SO 16+2+2)

DESCRIPTION

The L6374 is especially designed to be used as a line driver in industrial control systems based on the 24V signal levels (IEC1131, 24VDC).

BLOCK DIAGRAM



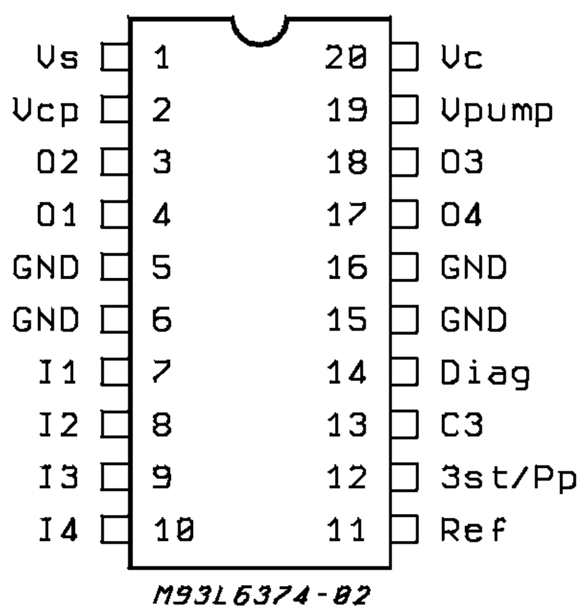
December 1994

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_S	1	Supply Voltage ($t_W \leq$ 10ms)	50	V
		Supply Voltage (DC)	40	V
V_{ilog}	12, 13	Logic Input Voltage (DC)	-0.3 to 7	V
I_{ilog}		Logic Input forced current, per pin	±1	mA
I_i	7, 8, 9, 10	Channel Input Current (forced)	±2	mA
V_i		Channel Input Voltage	- 7 to 35	V
I_{out}	3, 4, 17, 18	Output Current (forced, apart from inductive load)	±100	mA
		Output Current (forced, apart from inductive load) same $t_W \leq$ 10ms	±1	A
V_{out}		Output Voltage (forced, not resulting from an inductive kick)	-0.3 to V_S +0.3	V
I_{set}	11	Setting pin forced current	±1	mA
V_{set}		Setting pin forced voltage	-0.3 to 5	V
V_{diag}	14	External voltage	-0.3 to 35	V
I_{diag}		Externally forced current	-10 to 10	mA
V_{C3}	13	Voltage on the delay capacitor, externally forced	-0.3 to 4.5	V
T_{op}		Ambient temperature, operating range	-25 to 85	°C
T_j		Junction temperature, operating range (see Overtemperature Protection)	-25 to 125	°C
T_{stg}		Storage temperature	-55 to 150	°C

PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (V_S = 24V; T_j = -25 to 125°C; unless otherwise specified.)

DC OPERATION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	1	Supply Voltage		10.8		35	V
V_{sh}		UV UpperThreshold		9		10.8	V
H_{ys1}		UV Hysteresis		250	450	650	mV
I_{qsc}		Quiescent Current	Outputs Open		3	5	mA
V_{ref}	11	Input Comparators Reference Voltage	Reference pin Floating	1.05	1.25	1.35	V
I_{ref}		Sink/Source Current on Reference Pin	V_{ref} = 0V	-30	-20	-10	µA
			V_{ref} = 5V	10	20	30	µA
V_{th}	7, 8, 9, 10	Comparator Threshold with External Bias	V_S = 9 to 12V	-0.2		2.0	V
			V_S = 12 to 35V	-0.2		5.0	V
V_{il}		Input Low Level	V_{REF} Externally Biased	-7		V_{REF} -0.2	V
			Pin V_{REF} Floating	-7		0.8	V
V_{ih}		Input High Level	V_{REF} Externally Biased	V_{REF} +0.2		35	V
			Pin V_{REF} Floating	2		35	V
V_i		Input Voltage (Operative Range)		-7		35	V
I_{bias}		Input Bias Current	0 < V_i < V_S	-1		1	µA
			V_i = -7V	-1	-0.5	-0.1	mA
H_{ys2}		Input Comparators Hysteresis	See Analog Inputs Sections	100	200	350	mV
T_h		OVT Upper Threshold			170		°C
H_T		OVT Hysteresis			20		°C
I_{sc}	3, 4, 17, 18	Current Limit	V_i = -7 to V_S; V_{out} = 0 to V_S;	110	200	300	mA
V_{on}		Internal Voltage Drop @ Rated Current	I_{out} = ±100mA; Sourced @ High Output, Sunk @ Low Output T_j = 125°C		400	600	mV
			Same, T_j = 25°C		250	400	mV
I_{lkg}		Output 3-State Leakage Current	V_{out} = 0 to V_S	-25		25	µA
V_{in}	12	Push-Pull Mode Request		-0.2		0.8	V
		3-State Mode Request		2		5.5	V
I_{in}		Input Current	V_i = 0V		10	25	µA
I_{dlkg}	14	Diagnostic Output Leakage	Diagnostic Off; V_{diag} = 24V			5	µA
V_{diag}		Diagnostic Output Voltage Drop	I_{diag} =5mA		200	500	mV

AC OPERATION (V_S = 10.8 to 35V; T_j = -25 to 125°C; I_{out} = 100mA; unless otherwise specified; see switching waveforms diagrams)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{dr}	7 to 4 8 to 3 9 to18 10 to17	Delay Time on Rising Edge	R_l to ground		1000	1500	ns
			R_l to V_S		500	1000	ns
t_{df}		Delay Time on Falling Edge	R_l to ground		500	1000	ns
			R_l to V_S		1000	1500	ns
t_r	3, 4, 17, 18	Rise Time	R_l to ground		120	250	ns
			R_l to V_S		120	250	ns
t_f		Fall Time	R_l to ground		150	300	ns
			R_l to V_S		150	300	ns

THERMAL DATA

Symbol	Parameter	DIP20	SO20	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance, Junction to Pin	12	17	°C/W
$R_{th\ j\text{-}amb1}$	Thermal Resistance, Junction to Ambient (see Thermal Characteristics)	40	65	°C/W
$R_{th\ j\text{-}amb2}$	Thermal Resistance, Junction to Ambient (see Thermal Characteristics)	50	80	°C/W

THERMAL CHARACTERISTICS

$R_{th\ j\text{-}pins}$

POWERDIP. The thermal resistance is referred to the thermal path from the dissipating region on the top surface of the silicon chip, to the points along the four central pins of the package, at a distance of 1.5 mm away from the stand-offs.
SO. Similarly, the reference point is the knee on the four central pins, where the pins are upwardly bent and the soldering joint with the PCB footprint can be made.

$R_{th\ j\text{-}amb1}$

If a dissipating surface, thick at least 35 µm, and with a surface similar or bigger than the one shown, is created making use of the printed circuit.
Such heatsinking surface is considered on the bottom side of an horizontal PCB (worst case).

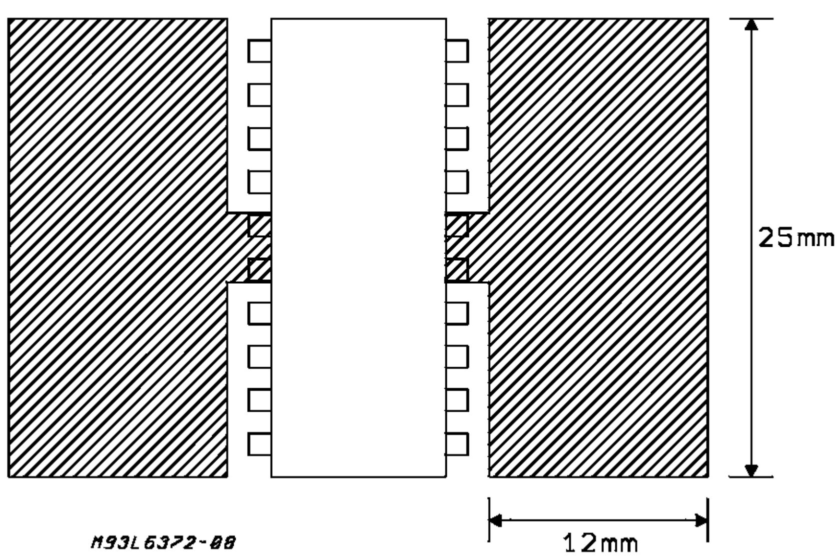
$R_{th\ j\text{-}amb2}$

If the power dissipating pins (the four central ones), as well as the others, have a minimum thermal connection with the external world (very thin strips only) so that the dissipation takes place through still air and through the PCB itself.
It is the same situation of point above, without any heatsinking surface created on purpose on the board.

Additional data for the PowerDip package can be found in:

Application Note 9030:
Thermal Characteristics of the PowerDip 20,24 Packages Soldered on 1,2,3 oz. Copper PCB

Figure 1: Printed Heatsink



SGS-THOMSON MICROELECTRONICS

OVERTEMPERATURE PROTECTION (OVT)

If the chip temperature exceeds T_h (measured in a central position in the chip) the chip deactivates itself.
The following actions are taken:

- all the output stages are forced in the "three state" condition, i.e. are disconnected from the output pins; only the clamping diodes at the outputs remain active;
- the signal Diag is activated (active low).

Normal operation is resumed as soon as (typically after some seconds) the chip temperature monitored goes back below T_h -H_T.
The different upper and lower thresholds with hysteretic behavior, assure that no intermittent conditions can be generated.

UNDERVOLTAGE PROTECTION (UV)

The supply voltage is expected to range from 11V to 35V, even if its reference value is considered to be 24V.
In this range the L6374 operates correctly.
Below 10.8V the overall system has to be considered not reliable.
Consequently the supply voltage is monitored continuously and a signal, called UV, is internally generated and used.
The signal is "on" as long as the supply voltage does not reach the upper internal threshold of the V_S comparator (called V_{sh}). The UV signal disappears above V_{sh}.
Once the UV signal has been removed, the supply voltage must decrease below the lower threshold (i.e. below V_{sh} -H_{ys1}) before it is turned on again.
The hysteresis H_{ys1} is provided to prevent intermittent operation of the device at low supply voltages that may have a superimposed ripple around the average value.
The UV signal inhibits the outputs, putting them in three-state, but has no effect on the creation of the reference voltages for the internal comparators, nor on the continuous operation of the charge-pump circuits.

DIAGNOSTIC LOGIC

The situations that are monitored and signalled with the Diag output pin are:

- current limit (OVC) in action; there are 8 individual current limiting circuits, two per each output, i.e. one per every output transistor; they limit the current that can be either sourced or sunk from each output, to a typical value of 150mA, equal for all of them;
- undervoltage protection (UV);
- overtemperature protection (OVP);

The diagnostic signal is transmitted via an open drain output (for ease of wired-or connection of several such signals) and a low level represents the presence of at least one of the monitored conditions, mentioned above.

PROGRAMMABLE DELAY

The current limiting circuits can be requested to perform even in absence of a real fault condition, for a short period, if the load is of capacitive nature or if it is a filament lamp (that exhibits a very low resistance during the initial heating phase).
To avoid the forwarding of misleading, short diagnostic pulses in coincidence with the intervention of the current limiting circuits when operating on capacitive loads, a delay of about 5µs is inserted on the signal path, between the "OR" of the current limit signals and its use as external diagnostic.
It takes about 1µs to charge (or discharge) by 24V a capacitor of 5nF with a current of 120mA .
To implement longer delays (from the intervention of one of the current limiting circuits to the activation of the diagnostic) an external capacitor can be connected between pin C3 and ground (pin C3 is otherwise left open).
The delay shall then be determined by the ratio of about 10 pF/µs, using the value of the capacitance connected to the pin.

ANALOG INPUTS (I1,I2,I3,I4)

The input stage of each channel is a high impedence comparator with built-in hysteresis (200mV) for high noise immunity. Each comparator has one input connected to all the others and tied to a common pin Ref (Pin 11). If this pin is left floating an internal precise band gap voltage reference (1.25V) is applied, otherwise these inputs can be externally programmed by connecting an external voltage source (from 0 to 5V) and the current on this pin is internally limited to ±20µA.
The other input pin of each comparator can swing from -7 to 35V.
For this reason it has been implemented the structure shown in Figure 2 and the device can also be used as line receiver.
When the input voltage is negative, the current is internally limited by a 15kΩ resistor as shown in Figure 2. High and low input thresholds can be obtained by adding and subtracting half of the hysteresis to the voltage of pin Ref (see Figure 3).

Figure 2: Equivalent input circuit

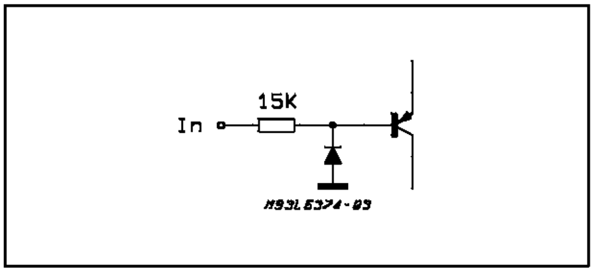
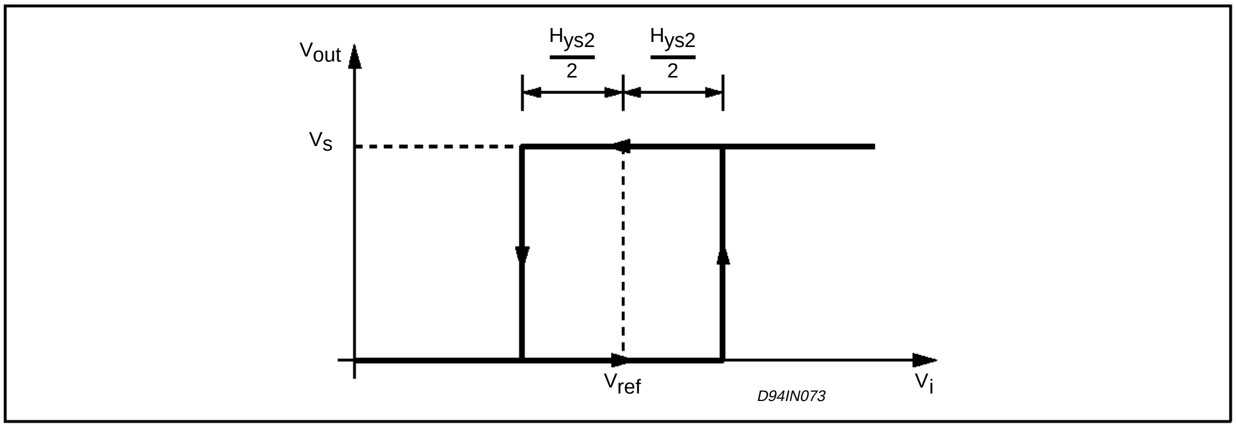


Figure 3: Input Comparator Threshold



3 STATE / PUSH-PULL INPUT

The input 3st/Pp is instead intended for a digital incoming signal. It has an internal threshold set at 1.26V; an internal bias circuit (10µA typical) simulates a high level (three-state) if the pin is disconnected.

THE SWITCHING OF THE OUTPUT STAGE

The cross conduction of the two transistors of an output stage of the L6374 would be significantly noisy, because the transistors here can carry peak currents in excess of 100mA, and even more in the few nanoseconds before the current limiting circuits are really effective.

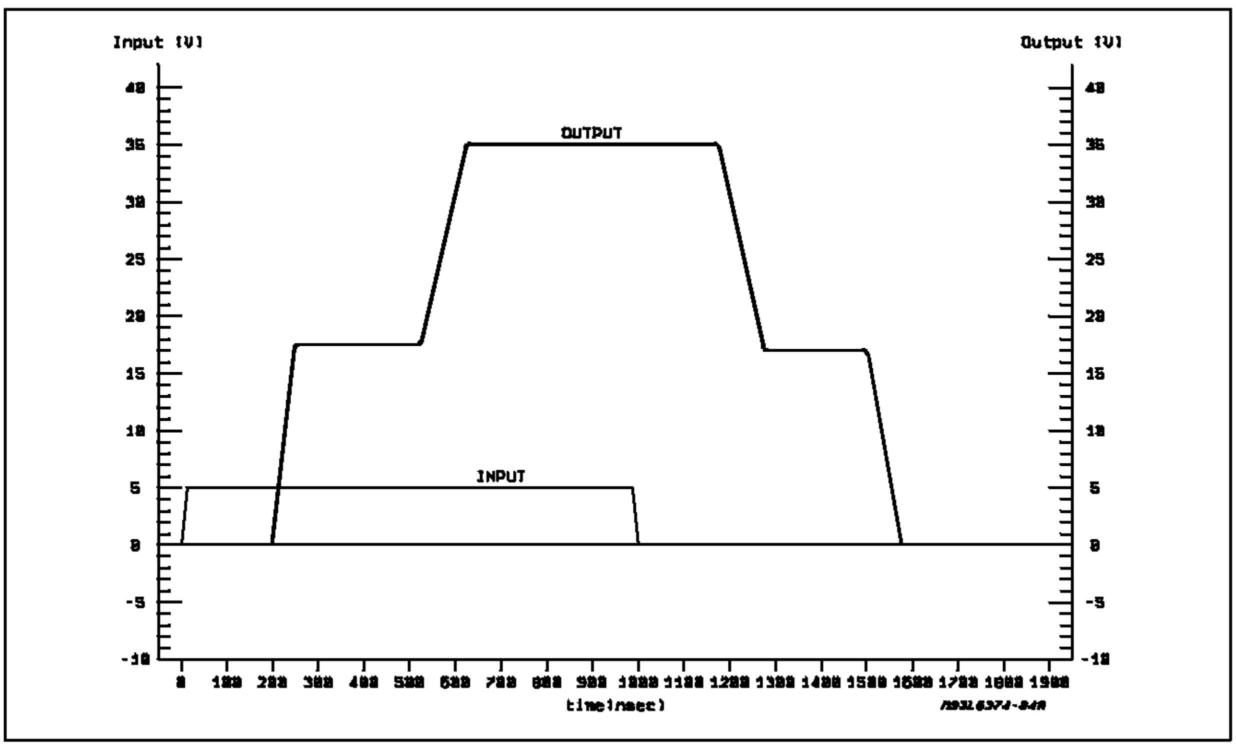
Consequently the device has been designed so as to avoid such cross conduction. At every switching transition, first of all the transistor in conduction is turned off. Then, after a safe interval of around 200ns, the other transistor is turned on.

When analyzing the switching cycle, and the associated switching times, it is useful to identify some subsequent phases:

- delay from the input pin to the output reaction;
- off transition in the output stage;
- dead time;
- on transition in the output stage.

Figure 4 helps understand such sequence. In

Figure 4: V_S = 35V, 350Ω connected to V_S/2.

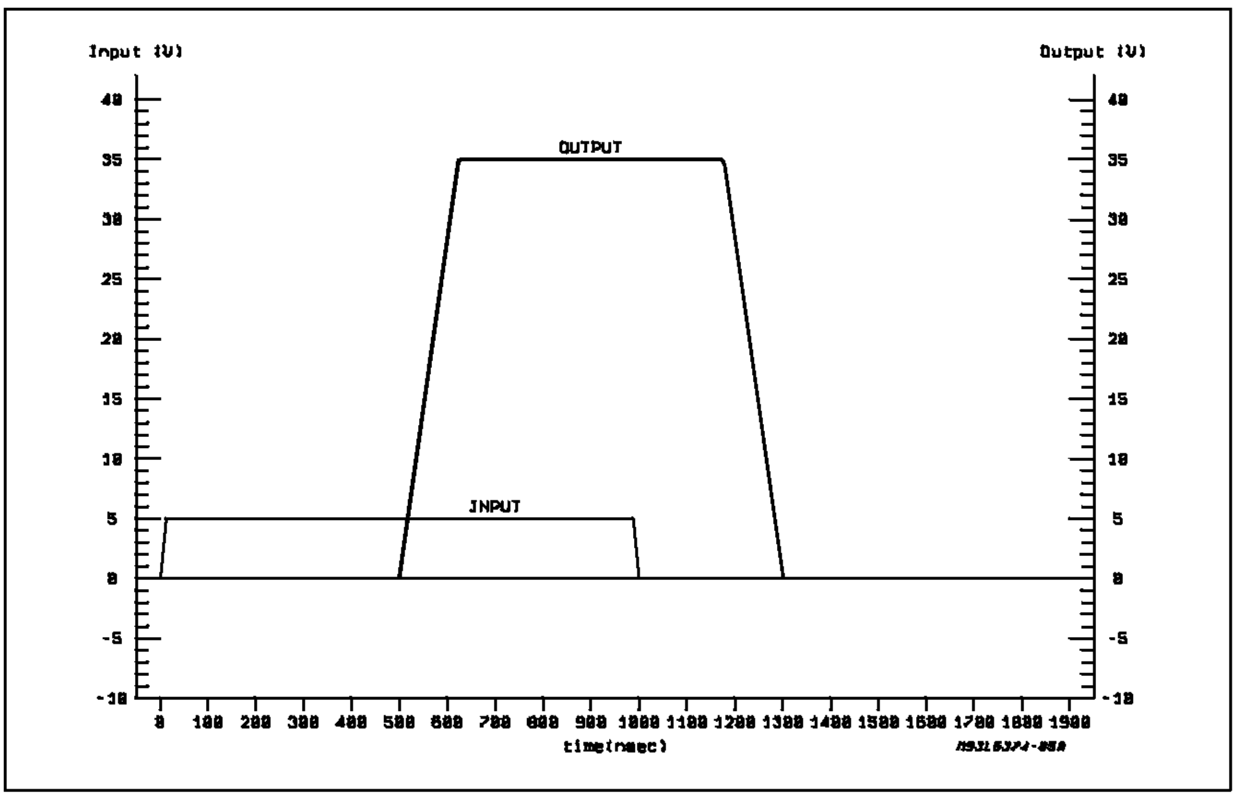


fact, with a purely resistive load connected to $V_S/2$ no parasitic elements interfere significantly.
The waveform can be significantly less easy to interpret if the load has not the perfect symmetry of that case, as showed below. For instance, it is enough to connect the resistive load to ground, or to V_S – as figure 5 and 6 – show to hide some of the switching phases described.

If the load is connected to ground, the waveform stays stuck to ground as long as the output stage is in high impedance; viceversa when the load is connected to V_S the waveform will linger close to the supply voltage as long as possible.
If an output load made of an inductor and a resistor in series is used, the inductive kick at the beginning of every output transition generates the equivalent effect of an "anticipated" switching when the inductor can discharge; while the switching looks "delayed" if the output transition tends to initiate a charging phase (see figure 7).
With a load almost free from parasitic elements, the waveforms resemble the ones of the purely resistive cases.
With a real, more composite load, the effect of the inductive kick in comparison to the resistive load, would be more apparent.
With a capacitor and a resistor in parallel as a load, another type of waveform can be seen (reported in figure 8).
As long as the output stage stays in the transient high impedance state, the output voltage will follow the classic exponential law of an RC relaxation.
As soon as the other transistor is switched on and takes charge, the waveform is quickly forcibly brought to its steady state value.
From the above it is possible to see how the switching times, inherently very fast, of the output stages, may be difficult to identify in a waveform if the output load is not accurately taken into consideration.

Figure 9 show typical switching waveform for inputs and outputs.

Figure 5: V_S = 35V, 350Ω connected to ground.



SGS-THOMSON MICROELECTRONICS

Figure 6. V_S = 35V, 350Ω connected to V_S.

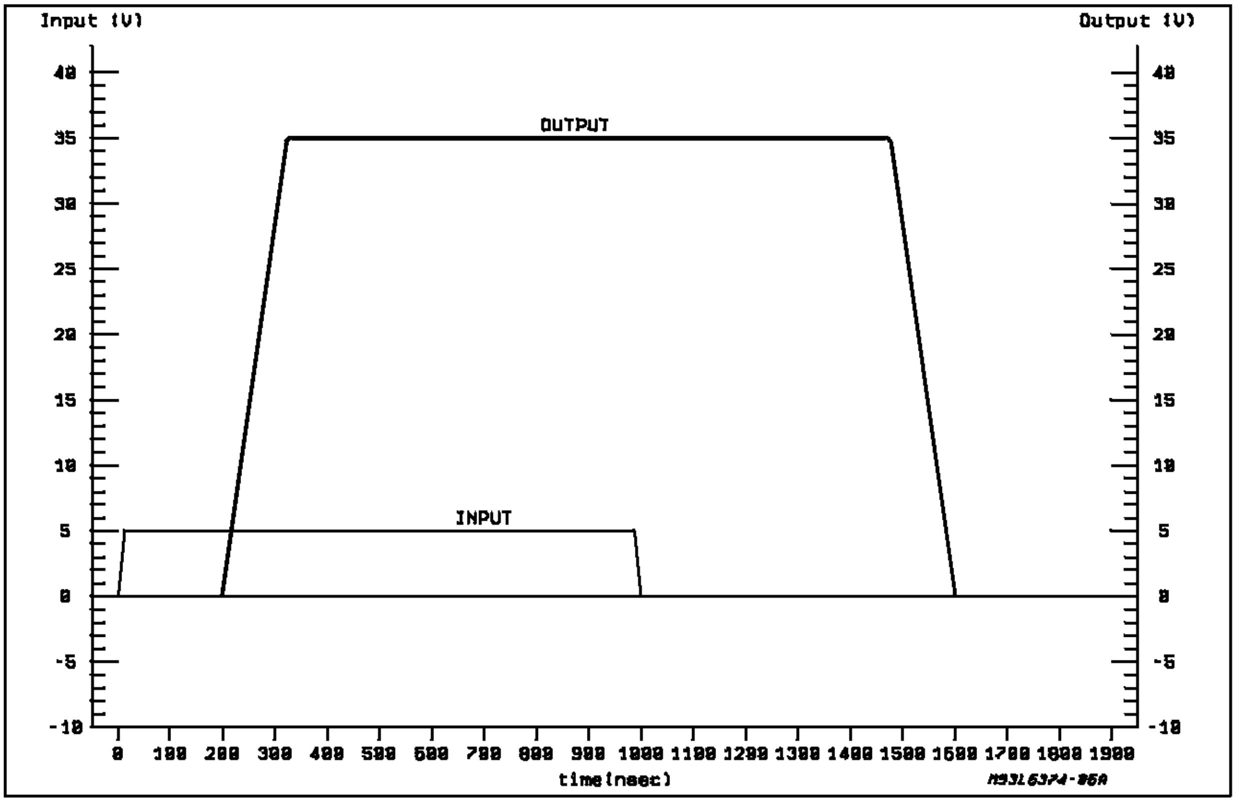


Figure 7. V_S = 35V, 350Ω & 1mH connected to ground.

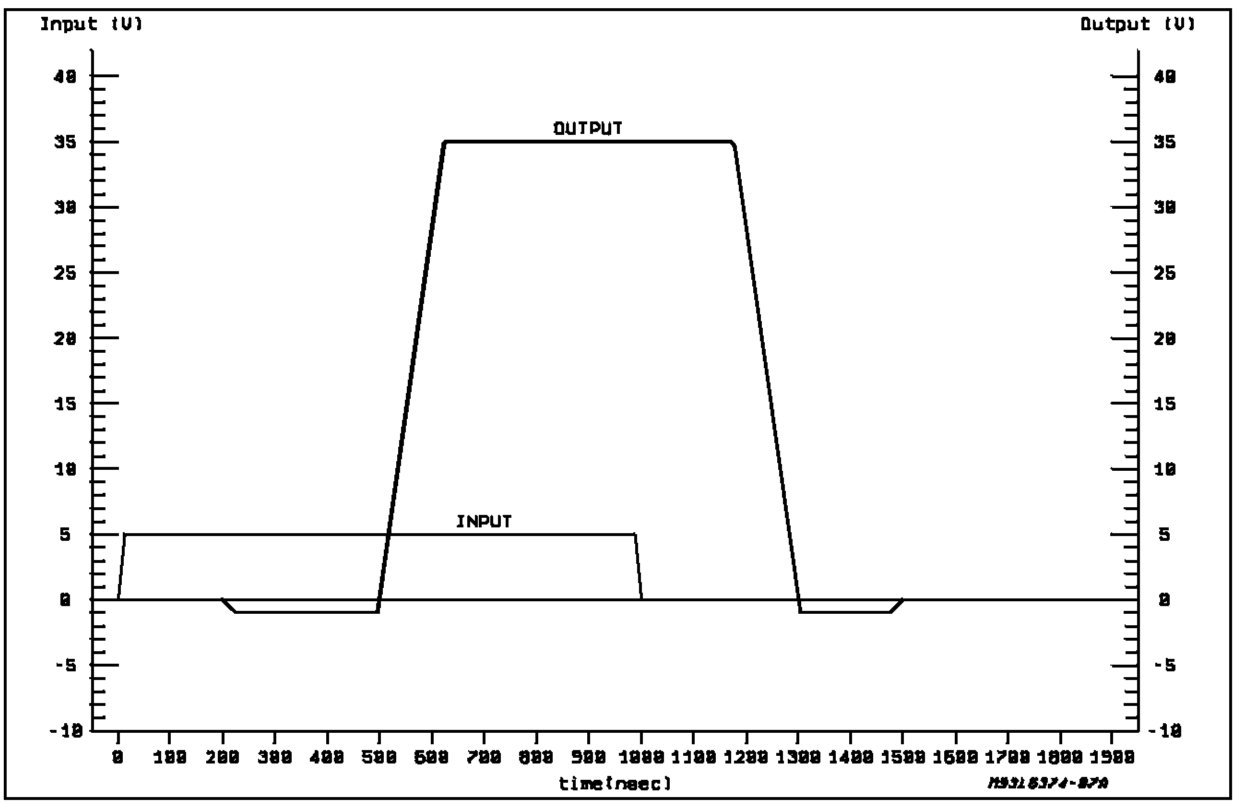


Figure 8: V_S = 35V, 350Ω || 1nF connected to ground.

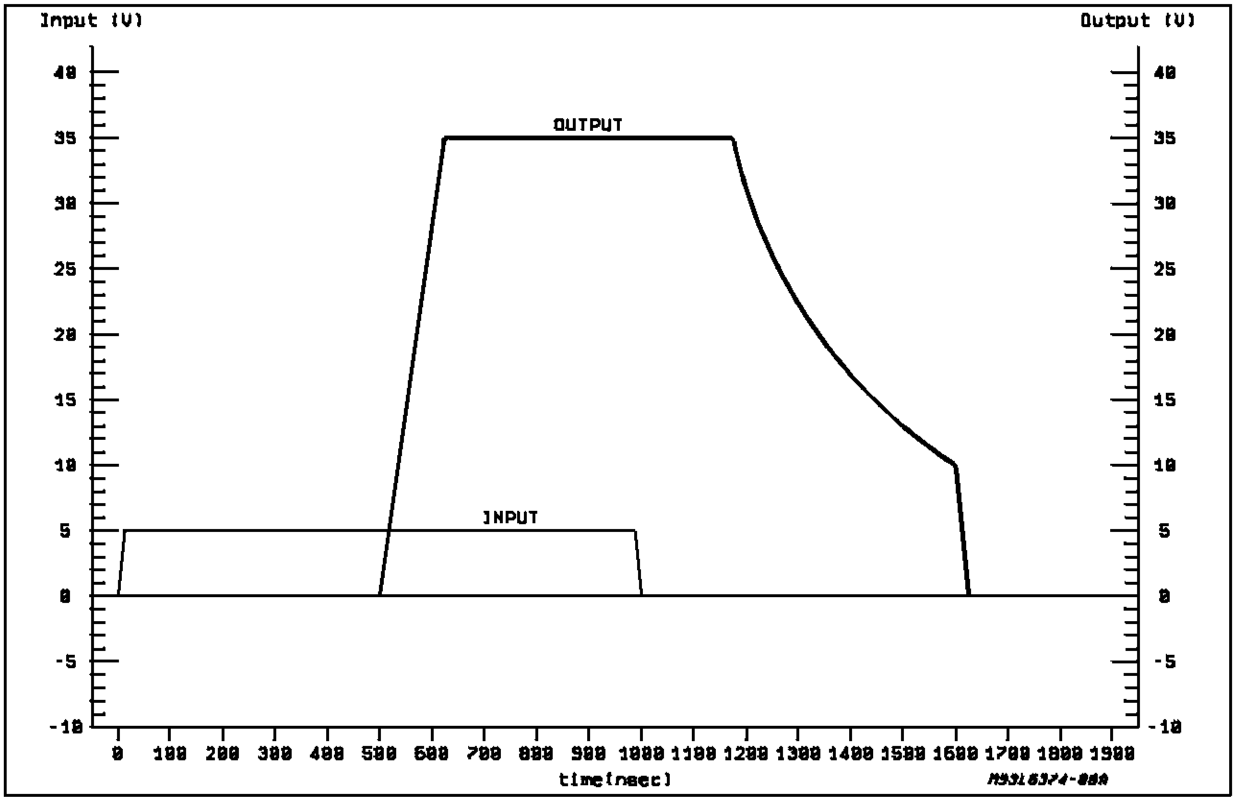
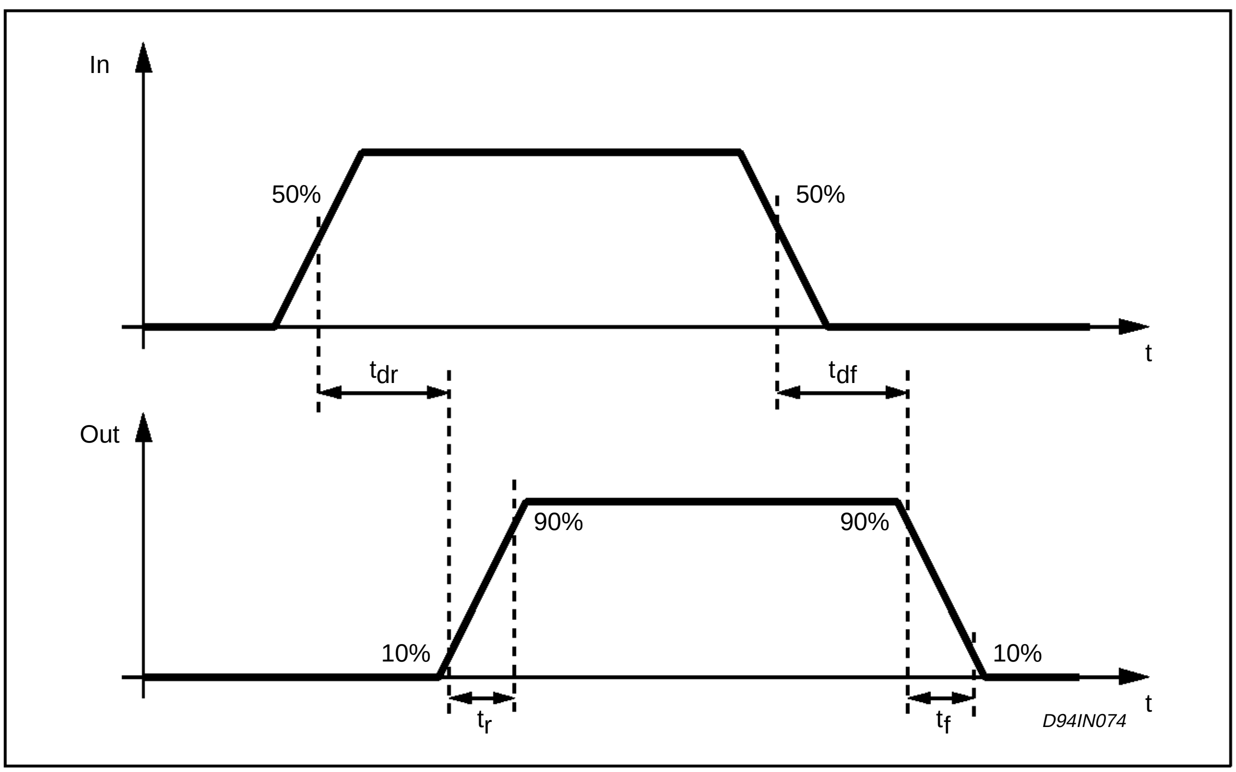


Figure 9: Switching Waveforms.



APPLICATION NOTE

It is recommended not to leave the Ref pin (pin 11) floating: if not used with an external voltage reference, it is better to connect an external capacitor (of at least 10nF) between this pin and ground.

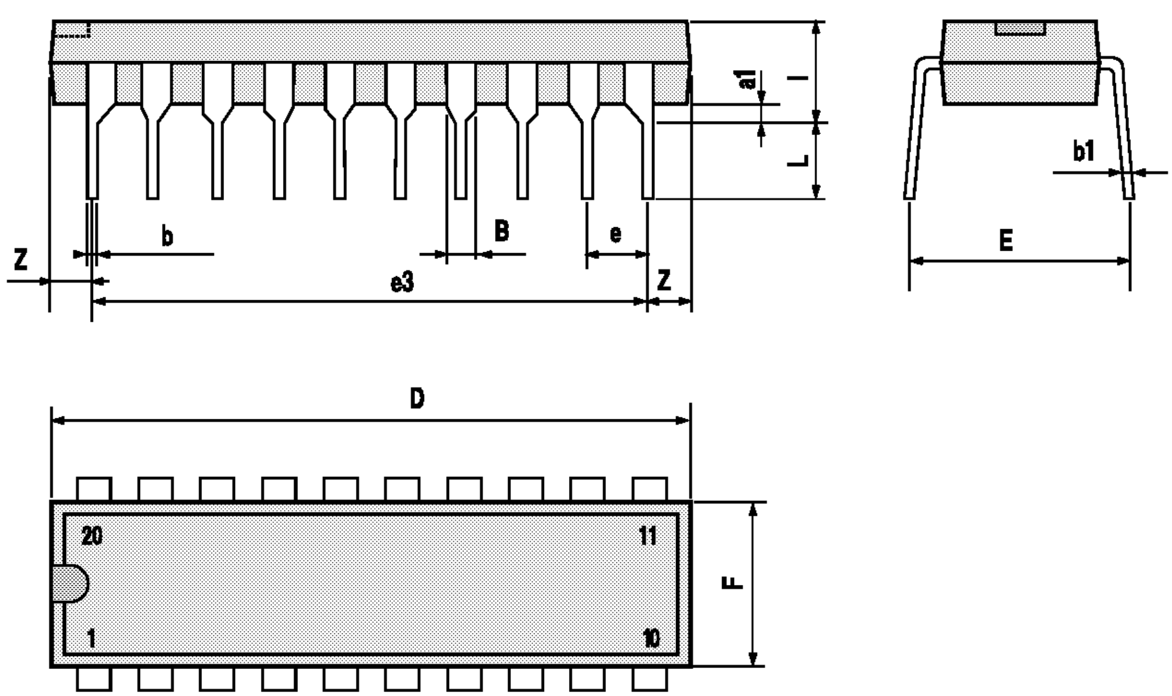
This capacitor filters the voltage reference against voltage spikes that can be generated by the commutation of the output stages.

This is very common using capacitive loads: in fact, the initial transient of such loads behaves like a short circuit, so the current flowing through the outputs presents very high spikes.

Moreover, if the device is used as a line receiver. (i.e. the input signals can go below ground) it is required not to leave the Ref pin (pin 11) floating: in this case, the pin can be connected to ground or to a fixed external voltage reference.

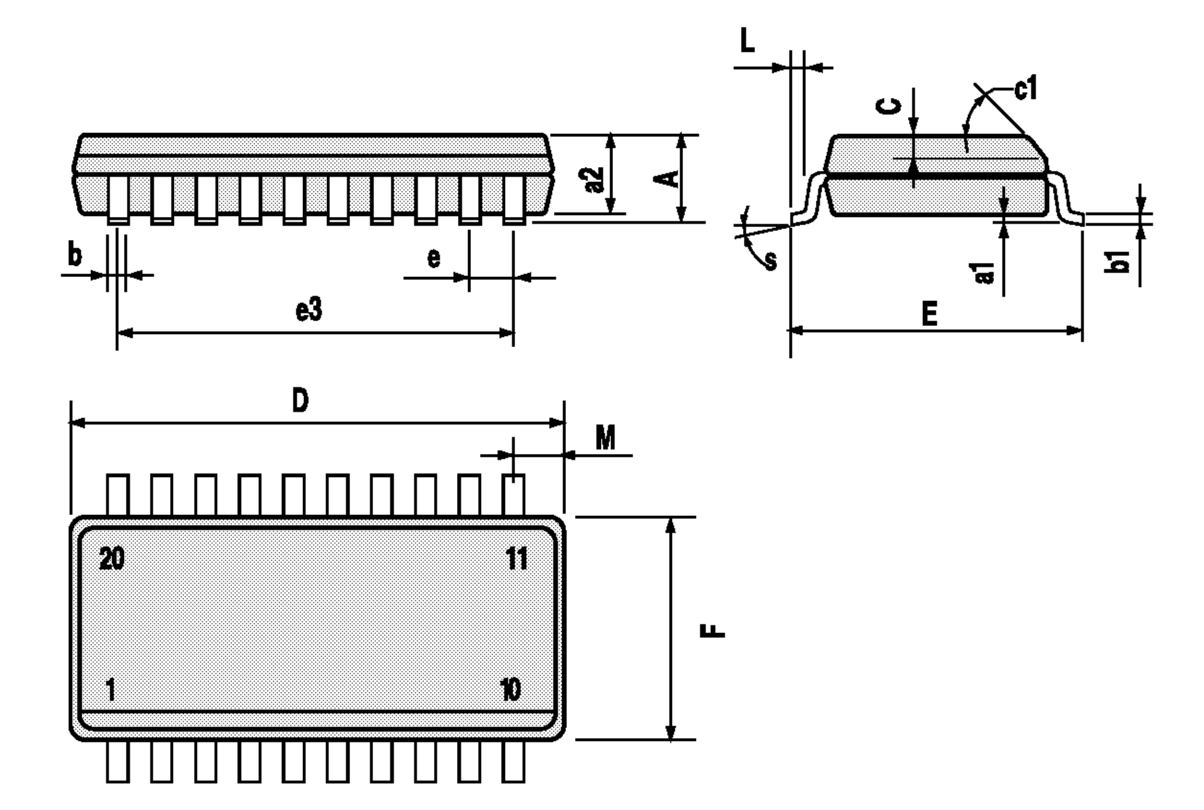
DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



SGS-THOMSON Microelectronics GROUP OF COMPANIES
Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands
Singapore - Spain - Sweden - Switzerland - Taiwan - Thaliand - United Kingdom - U.S.A.